REMARKS

The Office Action dated June 20, 2005, has been received and carefully considered. In this response, claims 2, 3, 6, 7, 13, 16, 17, 19 and 22-24 are amended to correct various informalities and to improve their consistency. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claims 13-23

The Applicant notes with appreciation the indication at page 4 of the Office Action that claims 13-23 were allowed. In this response, independent claims 13 and 22 are amended to provide better correspondence between the claim elements. In particular, the phrasing "one of the plurality... coupled to each of the plurality..." has been amended to "each of the plurality ... coupled to a respective one of the plurality..." As described in the specification, the discharge transistor is coupled to a corresponding bit line as follows:

> Column decode transistors 304[7:0] receive one of the first level column decode signals PREMUX[7:0], respectively. In addition, the inverses of PREMUX[7:0], that is, PREMUXB[7:0], are provided to discharge the NMOS transistors 306[7:0], respectively.... Discharge transistor 306[7] has a drain coupled to bit line BL[7], a gate coupled to PREMUXB[7], and a source coupled to V_{ss}...

See Application, page 5, paragraph 0024. Thus, the amendment is fully supported by the specification. None of the cited references suggest or disclose all the elements of amended claims 13 and 22, or claims 14-21 and 23 which depend from claims 13 and 22, respectively. Therefore, claims 13-23 remain in condition for allowance. Consideration and notice to that effect is respectfully requested.

Anticipation Rejection of Claims 1-5, 8-9, 12 and 23

At page 2 of the Office Action, claims 1-5, 8-9, 12 and 23 were rejected under 35 U.S.C. Section 102(b) as being anticipated by Hanriat et al. (U.S. Patent No. 6,282,114), hereinafter "the Hanriat patent". This rejection is hereby respectfully traversed.

As recited in claim 1 of the present application, the charging pulse is applied to a select one of the plurality of bit lines. The Office Action asserts:

> Regarding claims 1 and 23, Hanriat et al. disclosed in Figure 2 a ROM comprising a plurality of memory cells [MN] coupled between a plurality of word lines [W0-Wn] and a plurality of bit lines [BL], a plurality of reference cells (not shown)

> coupled to a reference bit line [DBL] (column 3, lines 5-10). A plurality of PMOS transistors [MP1, MP2] coupled between the bit lines [BL] and reference bit line [DBL] and high supply potential [Vdd] (column 2, line 66 to column 3, line 4). A plurality of NMOS transistors [MN1] coupled between the bit lines [BL], the reference bit line [DBL] and the low supply potential (ground) (column 3, lines 11-16). Hanriat et al. further disclosed in Figure 3 a timing diagram of a read operation of the ROM. A read signal [W], a clock signal [S] for sense amplifier [12], a [PUP] and [PDN] signals are generated by a sequencer [20] (column 3, lines 18-26). The [PUP*] signal is complement of signal [PUP] which is active when low, therefore, the signal [PUP*] is active when high (column 3, lines 27-31). In Figure 3, Hanriat et al. showed that as the read signal [W] goes low, which would be understood as the claimed inactive memory access period, the signal [PDN] becomes high and the transistors [MN1] is (sic) on to discharge the bit lines [BL] and the reference bit line [DBL]. As a read operation starts, *the selected bit line and the reference bit line is charging when the signal [PUP*] is high*, and the difference of voltage between the selected bit line [BL] and the reference bit line [DBL] is sensed by the sense amplifier [12] (column 3, lines 49-67).

Office Action, pp. 2-3 (emphasis added). Applicants respectfully disagree with the Examiner's characterizations that the selected bit line is charging when the signal [PUP*] is high.

In contrast to the present application, the Hanriat patent is directed to a low power-consumption read only memory (ROM), wherein transistors within the ROM are controlled using a common control line designated as "PUP" in FIG. 1. (*see* Col 3, lines 1-4). The common control line (PUP*, as relied upon by the Examiner) controls each of the transistors MP1, and each of the n-channel MOS transistors MN1 connects a respective bit line BL to the supply potential. (*see* Col. 3, lines 3-4 and lines 11-13). Thus, the charge signal on the PUP control line activates each of the transistors MN1, thereby charging all of the bit lines BL. (*see* FIG. 2). For example, each of the plurality of bit lines BL and the reference bit line (DBL) are charged by application of the PUP signal. (*see* Col. 3, lines 34-37). Thus, the charging signal is applied to all of the bit lines simultaneously, as opposed to applying the charging signal to a select one of the bit lines as recited in independent claim 1. Thus, the step of applying as recited in claim 1 is not suggested or disclosed in the Hanriat patent. The rejection of claim 1 over the Hanriat patent is therefore improper and should be withdrawn. Consideration and notice to that effect is respectfully requested.

Claims 2-5, 8-9 and 12 depend from allowable independent claim 1. Therefore, the rejection of claims 2-5, 8-9 and 12 over the Hanriat patent is improper, at least by virtue of their

dependency from claim 1, and should be withdrawn. Consideration and notice to that effect is respectfully requested.

Applicant notes that claim 23 was also rejected under 35 U.S.C. 102(b) as being anticipated by the Hanriat patent. However, at page 4 in paragraph 7, claim 23 is indicated to be allowed. Since claim 23 is dependent from allowed independent claim 22, it is assumed that the rejection of claim 23 was in error. Confirmation of the status of claim 23 is respectfully requested.

In the event that the rejection under section 102(b) was intended to be applied to independent claim 24, applicant notes (based on the discussion presented above) that the Hanriat patent fails to suggest or disclose "applying a charging pulse on a *selected one* of the plurality of bit lines" (emphasis added) as recited in claim 24. Instead, the Hanriat patent discloses applying a charging signal to all of the bit lines BL and to the reference line DBL. Thus, the invention as recited in claim 24 is not anticipated by the cited reference. Consideration and notice to that effect is respectfully requested.

Upon review of the claims, the Applicants detected a typographical error that is repeated in claims 2, 3, 16, 17, 19, 23 and 24. Specifically, the term "during" was omitted from each of the above claims, resulting in a grammatical error. Additionally, claim 24 included an additional typographical error wherein the term "delay" was repeated. With this response, claims 2, 3, 16, 17, 19, 23 and 24 are amended to correct the typographical errors.

In view of the foregoing, it is respectfully submitted that the Office Action fails to establish that the Hanriat patent discloses or suggests each and every element of claims 1-5, 8-9, 12 and 23 (or 24). It is respectfully submitted that the anticipation rejection of claims 1-5, 8-9, 12 and 23 (or 24) is improper at this time, and therefore withdrawal of this rejection is requested.

Obviousness Rejection of Claims 6-7

At page 4 of the Office Action, claims 6-7 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over the Hanriat patent. This rejection is hereby respectfully traversed.

In particular, the Office Action reads as follows:

> Hanriat disclosed the voltage difference is approximately 50 mV (column 4, lines 28). It would have been obvious to a person of ordinary skill in the art at the time

> the invention was made to modify the ROM of Hanriat et al. by selecting the voltage difference in the range of greater than or equal (sic) 100 or 150 mV.The rationale is as follows: A person of ordinary skill in the art would have been motivated to select the voltage difference in the range of greater than or equal 100 or 150 mV to obtain an accurate reading operation."

(*Office Action*, p. 4, paragraph 5). Claims 6 and 7 depend from claim 1. As previously discussed, the Office Action fails to establish that the Hanriat patent discloses or suggests each and every element of claims 1. For example, the Hanriat patent does not suggest or disclose applying a charging pulse on a selected one of the plurality of bit lines, as recited in claim 1. Instead, the Hanriat patent discloses applying a charging pulse to all of the bit lines. It would not have been obvious to a worker skilled in the art to modify the Hanriat patent to charge only a selected one of the plurality of bit lines as recited in claim 1, and there is no suggestion in the cited reference to make such a modification. Thus, the Hanriat patent fails to suggest or disclose all of the elements of independent claim 1.

In view of the foregoing, it is respectfully submitted that the Office Action fails to establish that the Hanriat patent discloses or suggests each and every element of claims 6 and 7, which depend from independent claim 1. It is respectfully submitted that the obviousness rejection of claims 6 and 7 is improper at this time, and therefore withdrawal of this rejection is requested.

Objection to Claims 10-11

At page 4 of the Office Action, claims 10-11 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claims. Applicant respectfully thanks the Examiner for the indication of allowability of claims 10 and 11 if rewritten. However, as discussed above, the Office Action fails to establish that the Hanriat patent discloses every element of independent claim 1, from which claims 10 and 11 depend. Therefore, the Office Action fails to establish that the Hanriat patent discloses every element of claims 10 and 11. Accordingly, the objection to claims 10 and 11 is improper at this time, and withdrawal of the objection to claims 10-11 is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is respectfully requested. The Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below if such a call would in any way expedite resolution of any issues to facilitate passage of the present application to issue.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

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Date

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